

Project Name : A14IM01_DDR3 X2

Platform : Montevina Penryn(CPU)+Cantiga(NB)+ICH9M(SB)

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M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

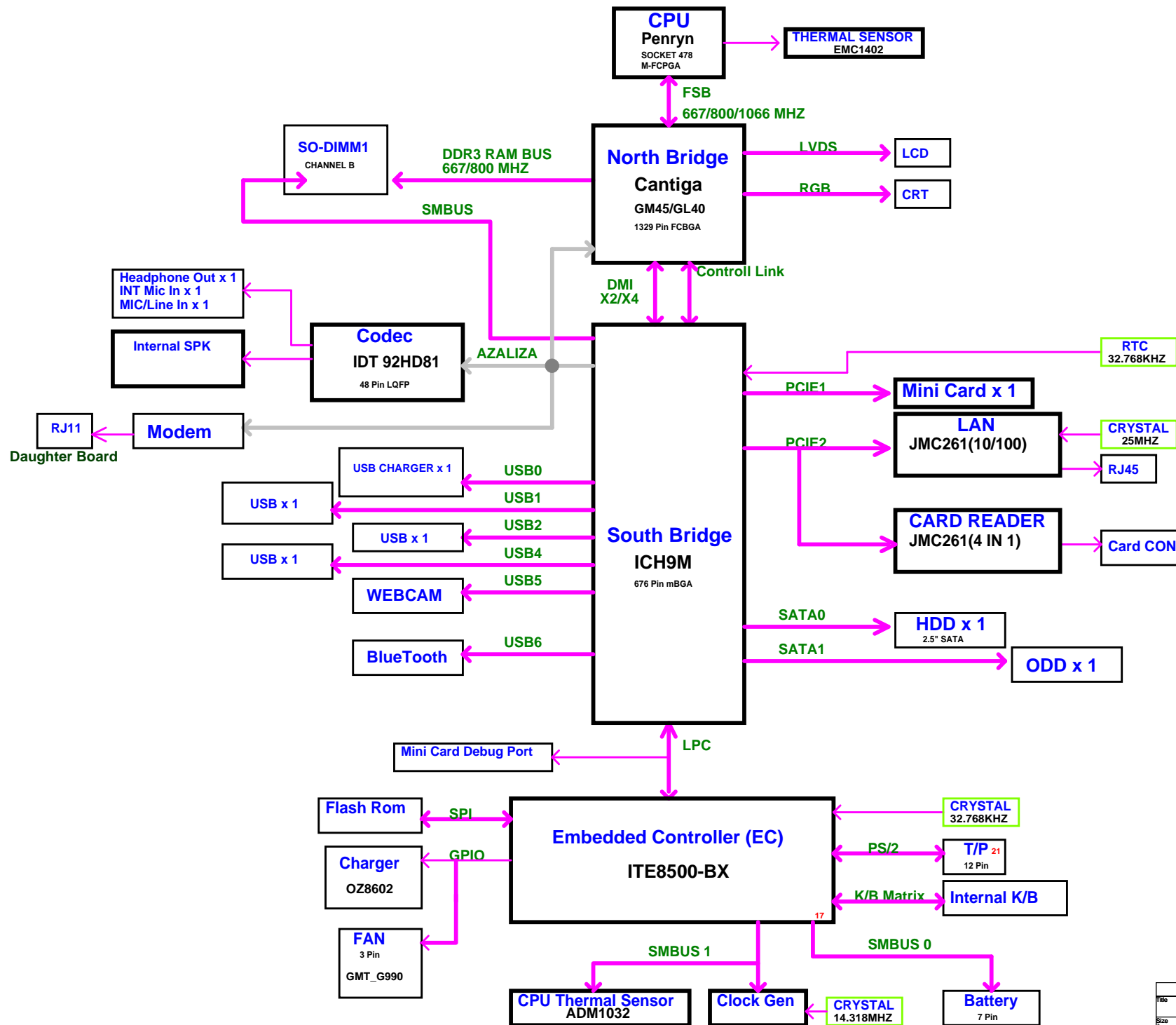
A14IMXX M/B V3.0 2 X DDR3 (02 SLOT DDR3)

71R-R14IM0-T830

Esquemático REV B

A14IMXX A14IM01

A14IM01 SYSTEM BLOCK DIAGRAM



500ms(min)



3



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	N.C (TACH3)
GPIO8	N.C
GPIO9	N.C (WOL_EN)
GPIO10	N.C (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	N.C (GLAN_DOCK#)
GPIO14	N.C (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	N.C (TACH0)
GPIO18	N.C
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	N.C (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	N.C (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8510 GPIO		Default Pull/Mode
GPA0	RF_LED#	UP / GPI
GPA1	EC_BSEL1	UP / GPI
GPA2	BT_L_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	P_ID0	UP / GPI
GPA5	P_ID1	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	+1.05V_ON	Dn / GPI
GPB3	BAT_SMBCLK	/ GPI
GPB4	BAT_SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	ENHANCE_USB#	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	N.C	Dn / GPI
GPC4	SAVE_POWER	Dn / GPI
GPC5	SLP_S4_COY	Dn / GPI
GPC6	+3.3VS_ON	Dn / GPI
GPC7	CRT_DETECT	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	N.C	UP / GPI
GPD4		UP / GPI
GPD5	PWR_USB_LED#	UP / GPI
GPD6	N.C	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	Fastcharge_EN	Dn / GPI
GPE2	PWROK	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	+1.2VS_ON	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	N.C	UP / GPI
GPF1	N.C	UP / GPI
GPF2	N.C	UP / GPI
GPF3	CHG_ON#	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	N.C	UP / GPI
GPF7	N.C	UP / GPI
GPG0	+3.3VA	Dn/GPO/TM
GPG1	+5V_ON	Dn/GPO/ID7
GPG2	N.C	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	SAFETY_PROTECT	Dn/GPI/ID0
GPH1	+1.8VS_ON	Dn/GPI/ID1
GPH2	SENBAT_V	Dn/GPI/ID2
GPH3	CHG_G_LED	Dn/GPI/ID3
GPH4	CHG_R_LED	Dn/GPI/ID4
GPH5	BATOFF	Dn/GPI/ID5
GPH6	PWR_LED	Dn/GPI/ID6

ITE8510 GPIO		Default Pull/Mode
GPI0	N.C	/GPI/ADC
GPI1	LCDSW0	/GPI/ADC
GPI2	LCDSW1	/GPI/ADC
GPI3	N.C	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PM_THROTTLING#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP(℃)
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP(℃)
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

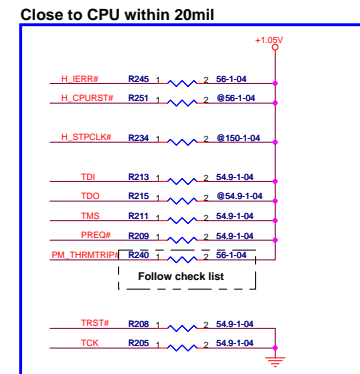
ITE8500			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	1000	3300	70

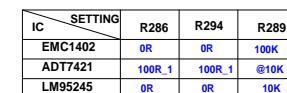
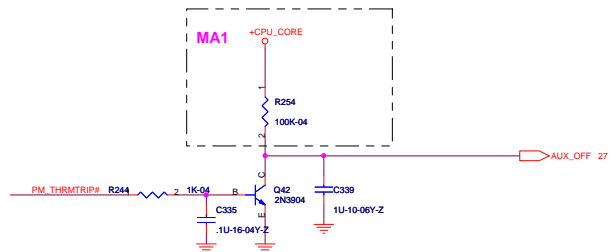
IDT92HD81			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP(℃)
+3.3V	170uA	0.56	150

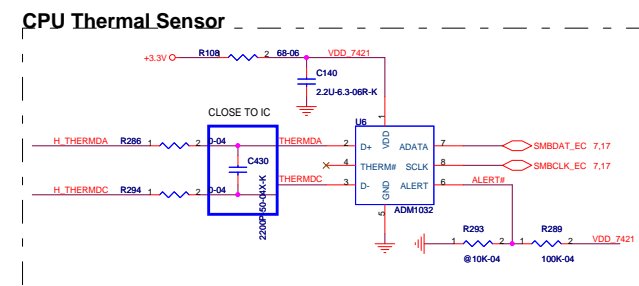
JMC261			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	300	990	70
+1.2VS	150	180	

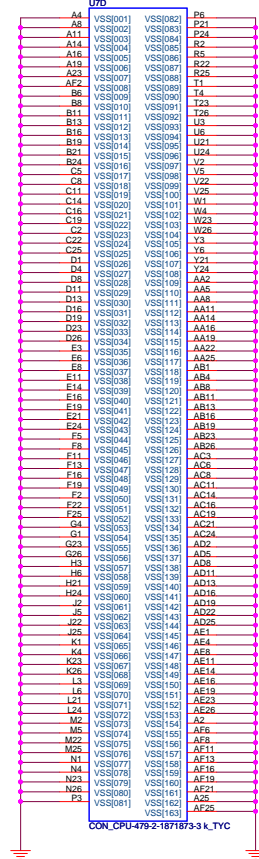
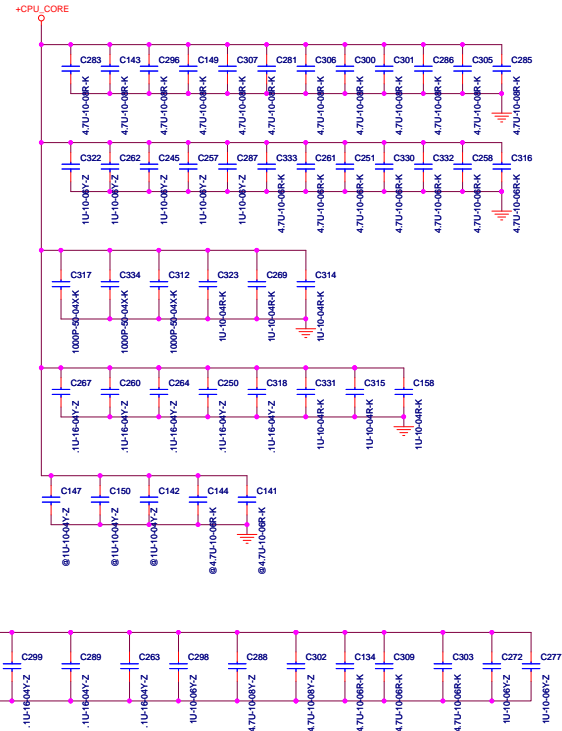
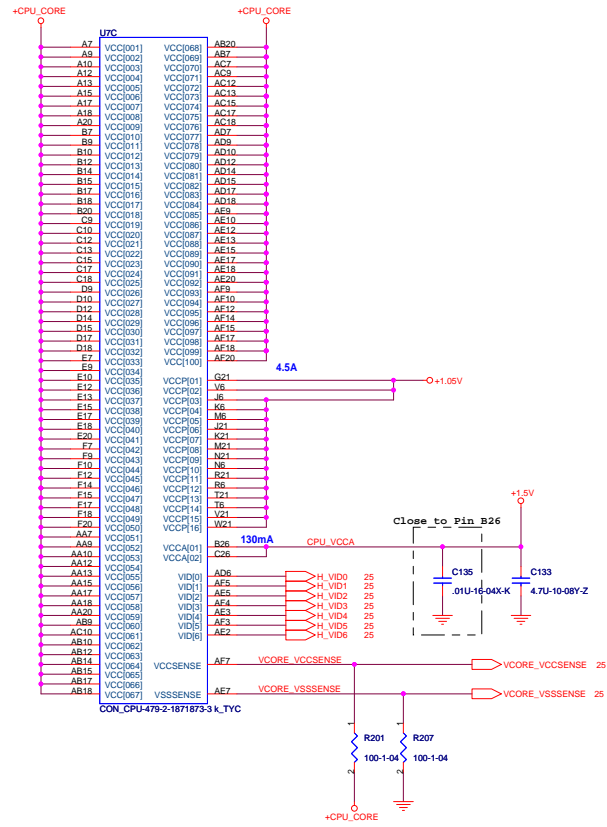


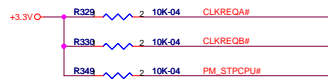
FSB \ BSEL	BSEL2	BSEL1	BSEL0	MHZ
FSB667	0	1	1	166
FSB800	0	1	0	200
FSB1066	0	0	0	266



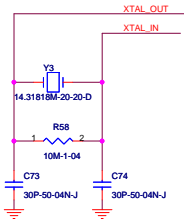
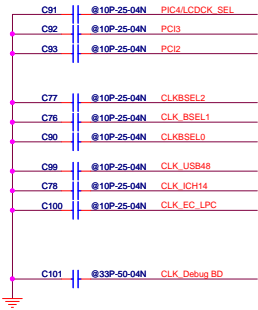
R289 can use 100K for 3 vender real application
R286,R294 can use 0-04 for ADT7421 real application



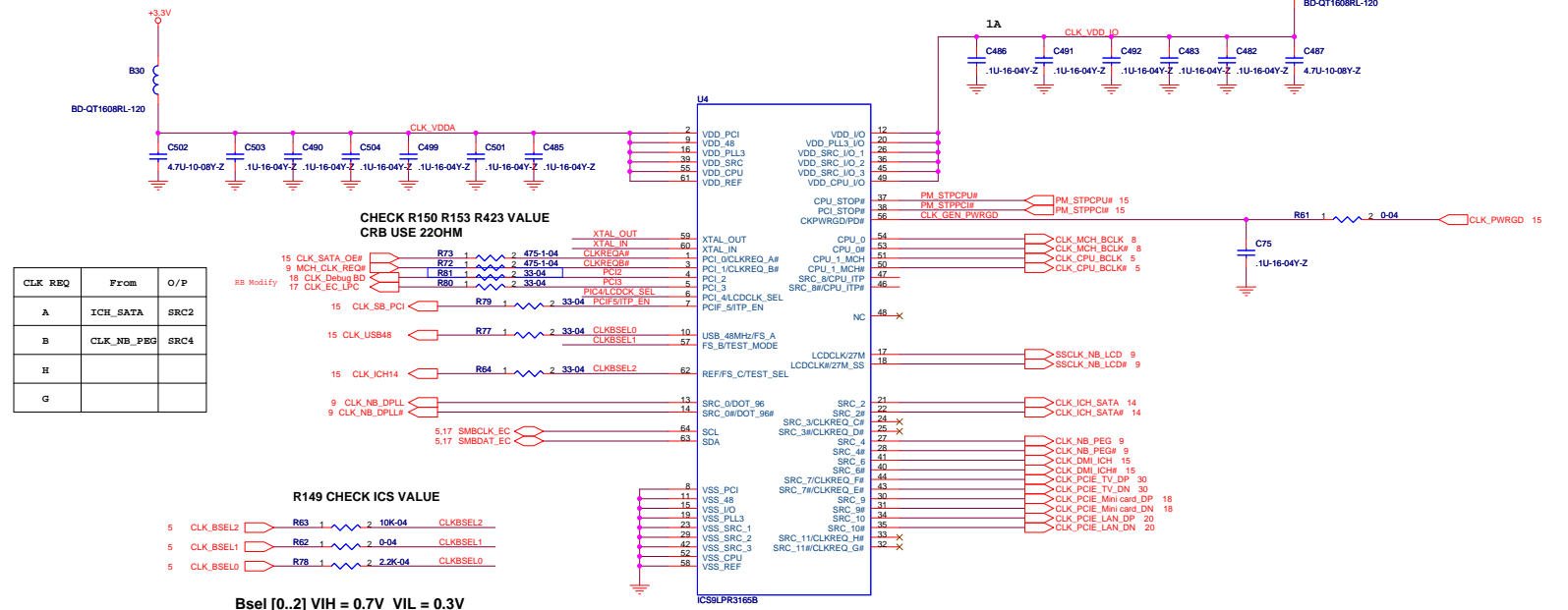




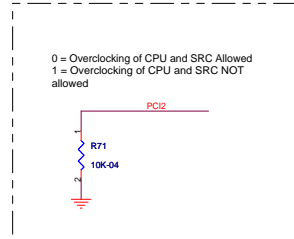
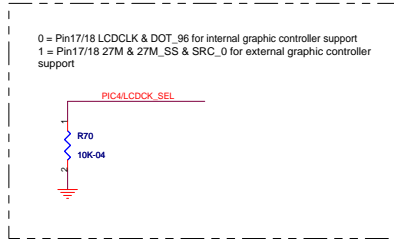
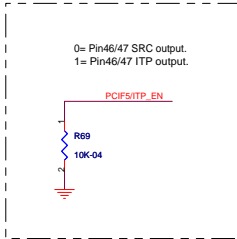
Reserved FOR EMI

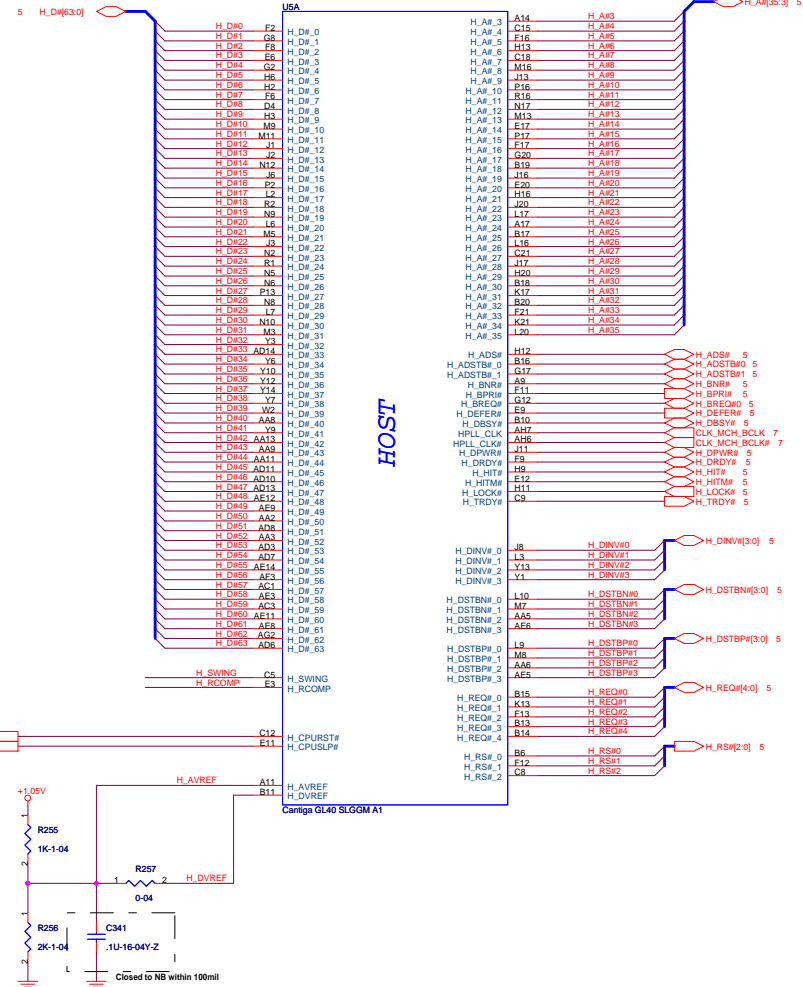
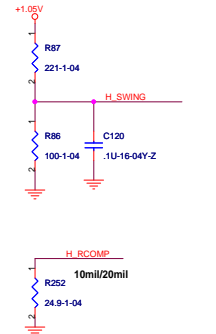
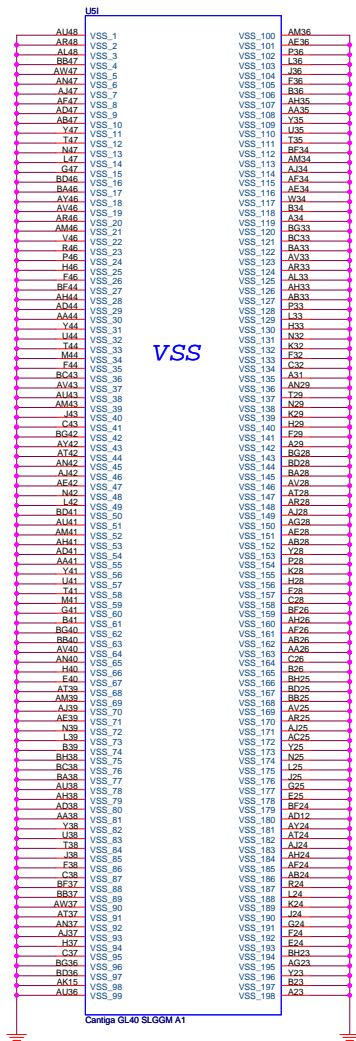


$C_e = 2 * CL - (C_s + C_i)$
 CL = Crystal Load Cap = 20P
 C_i = IC internal Cap = 5P
 C_s = 2P
 C_e = Crystal external Cap = 33P

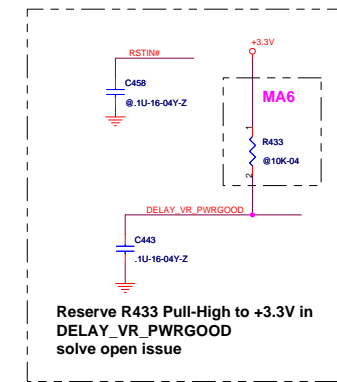
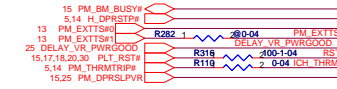


"Need reserved space for 72Pin CLOCK GEN"





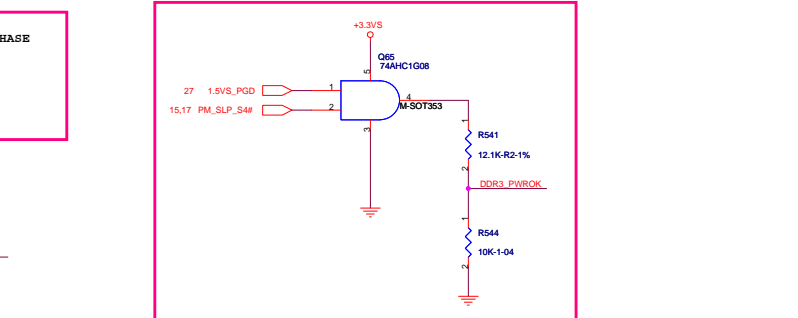
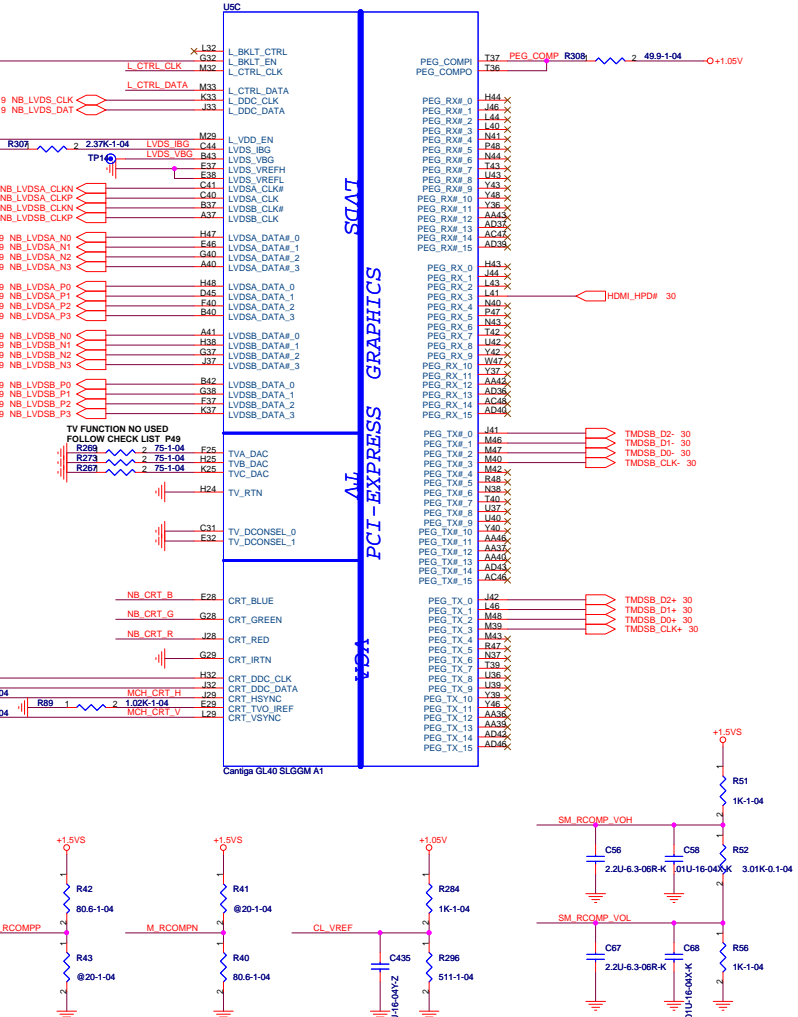
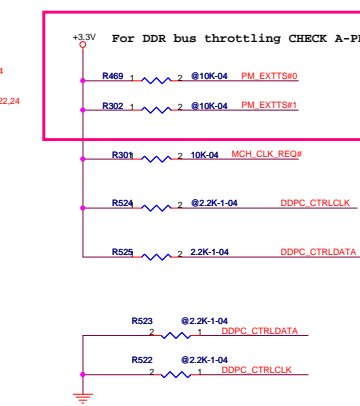
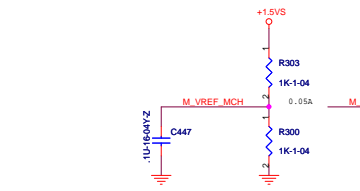
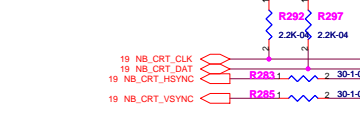
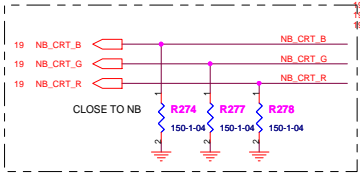
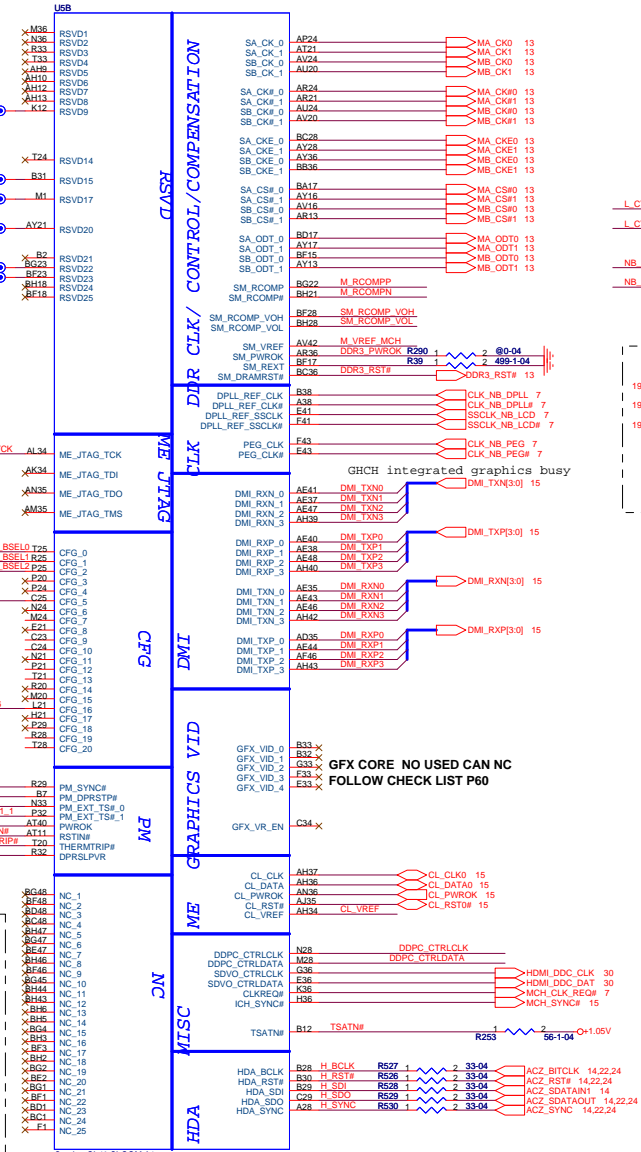
CHECK NB TABLE FOR INTEL

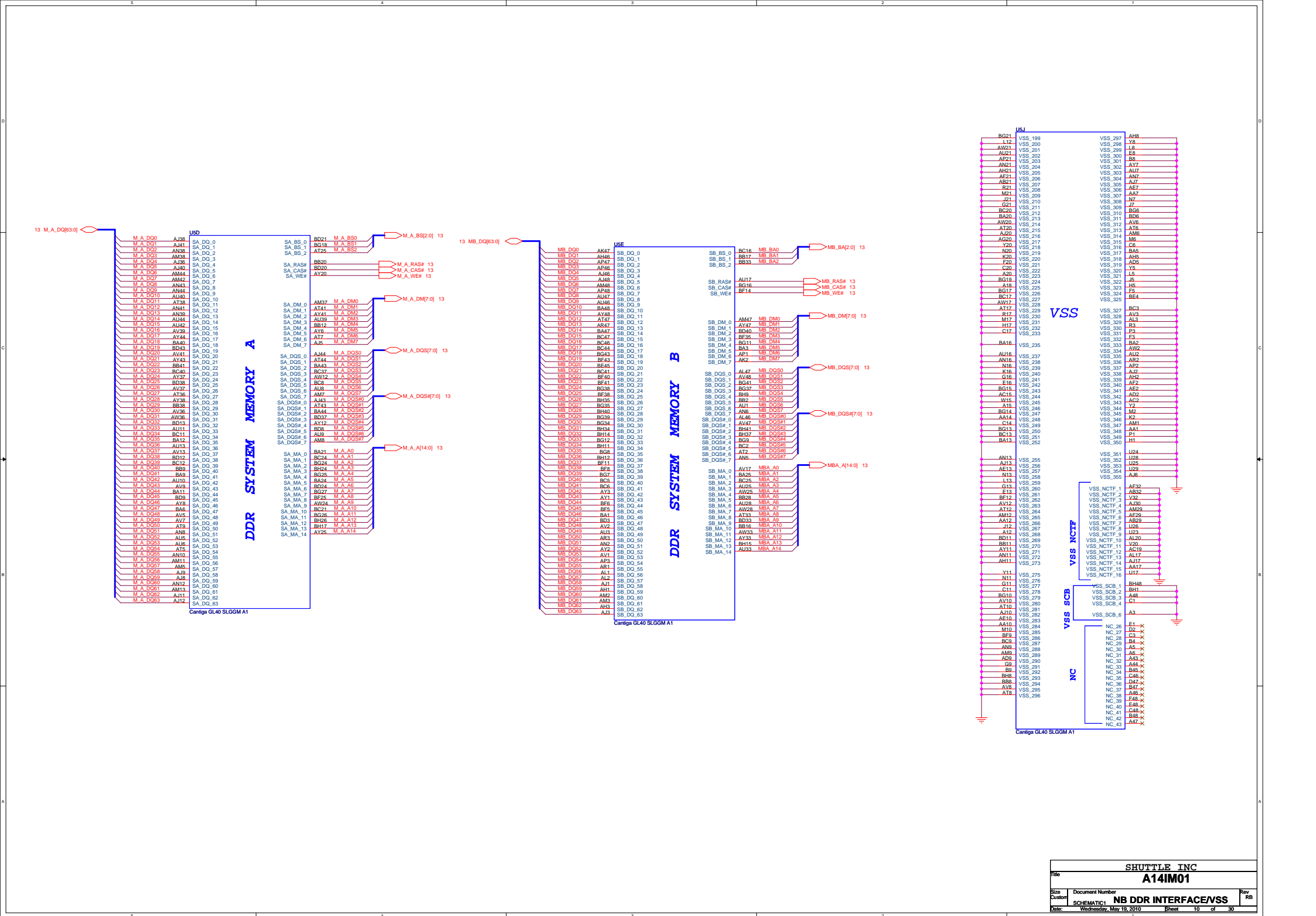


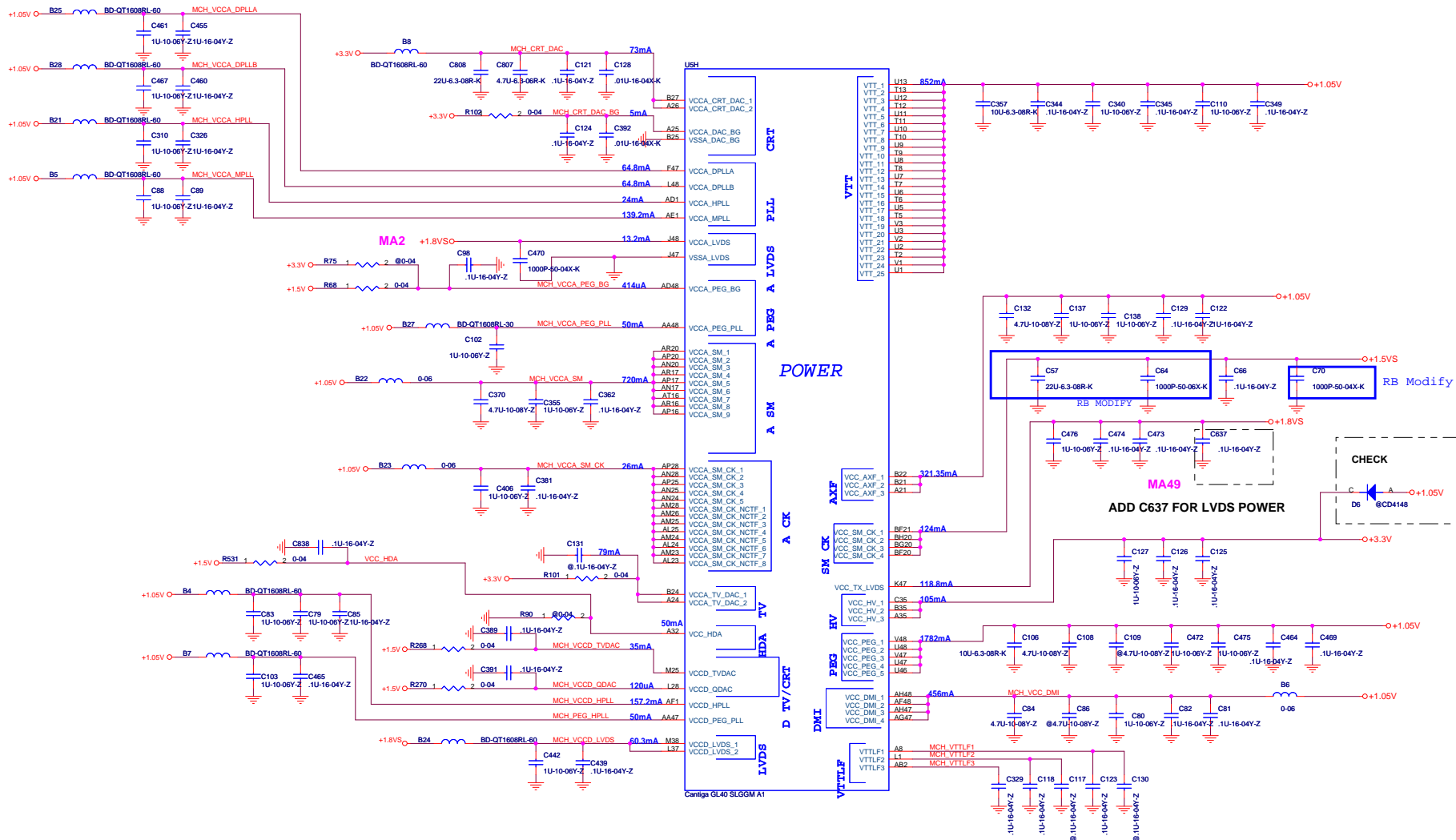
**Reserve R433 Pull-High to +3.3V in
DELAY_VR_PWRGOOD
solve open issue**

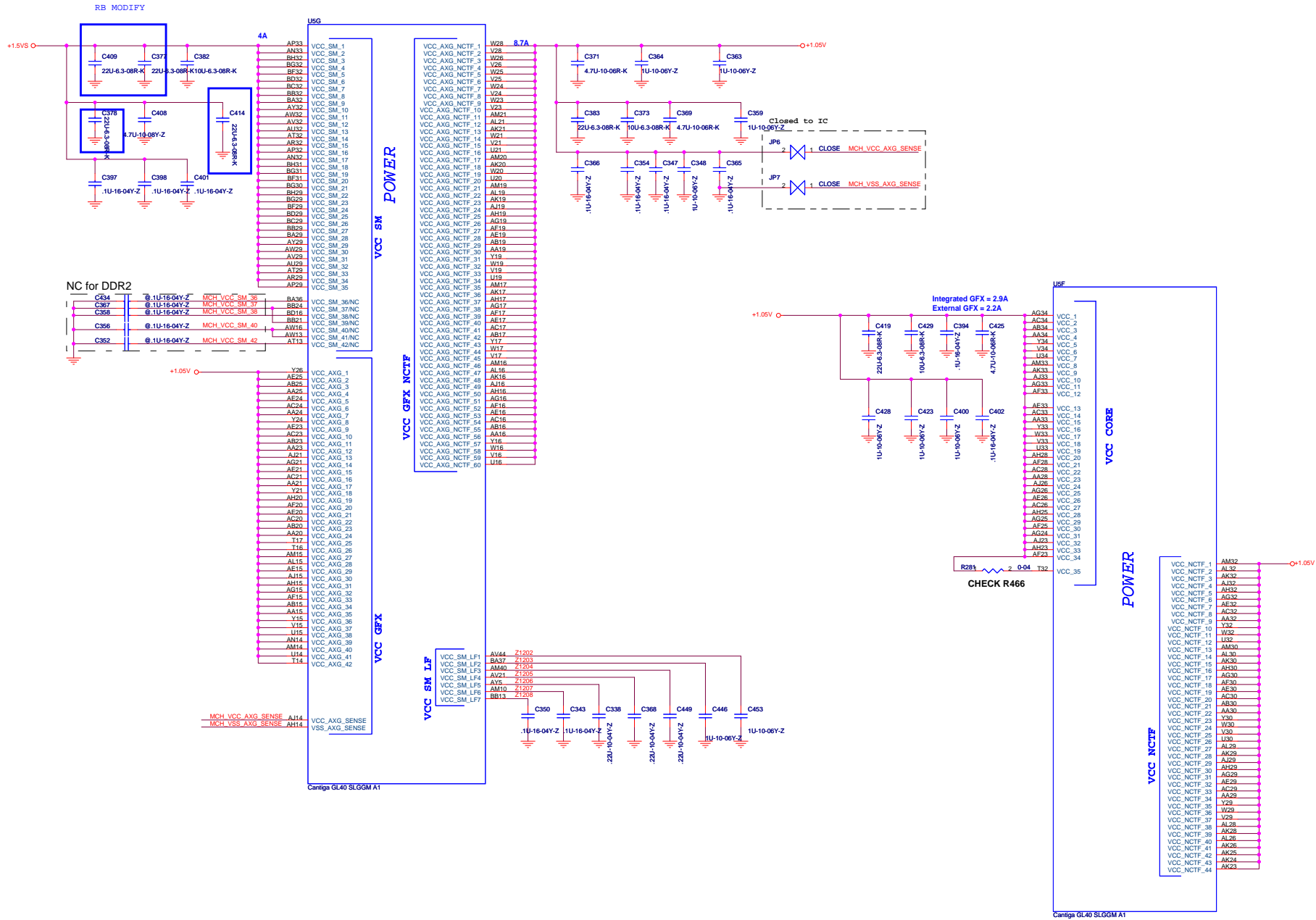
DMI X2 Select	
MCH_CFG5	0 = DMIx2
	1 = DMIx4 ★

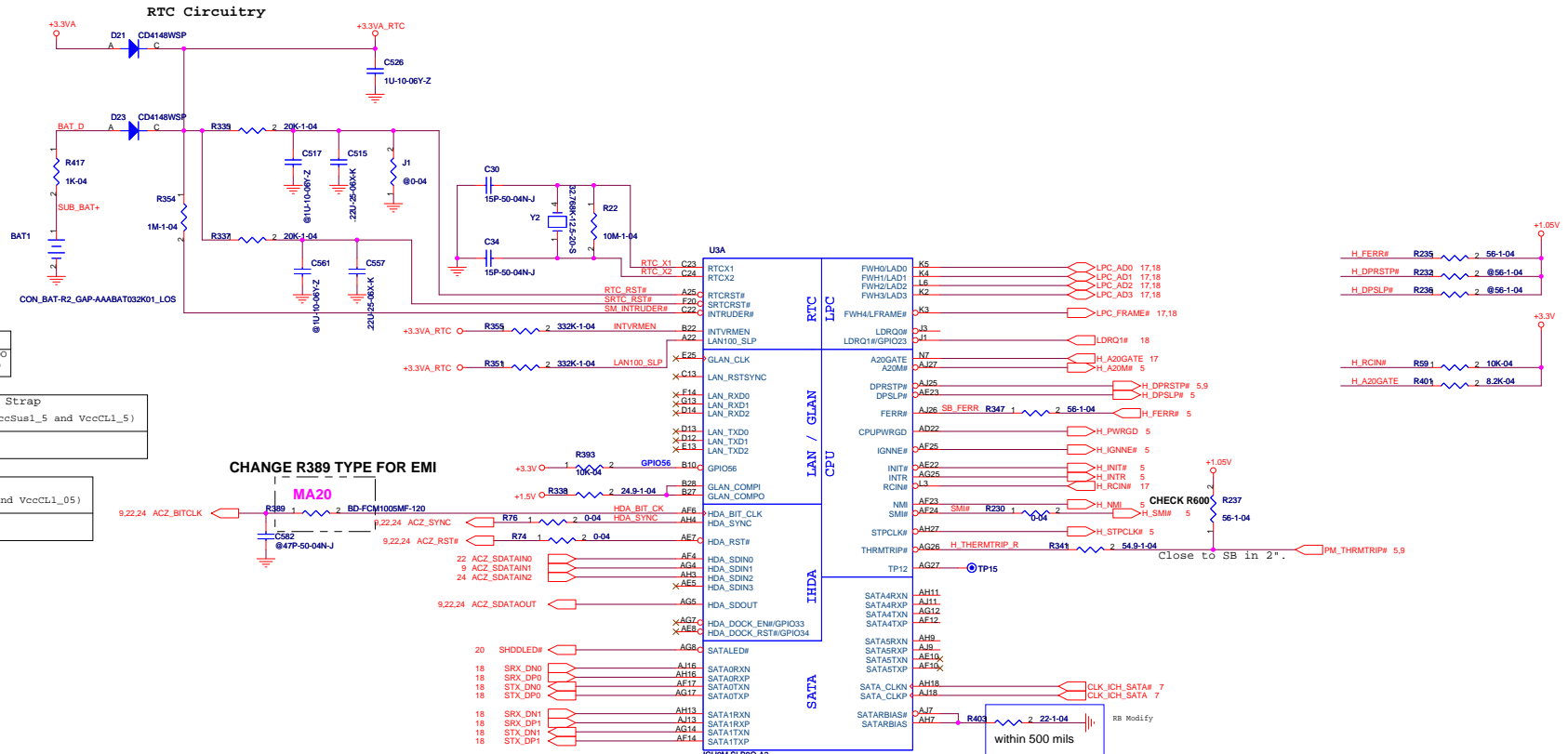
FSB Dynamic ODT	
MCH_CFG16	0 = Dynamic ODT Disabled
	1 = Dynamic ODT Enabled *

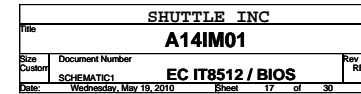




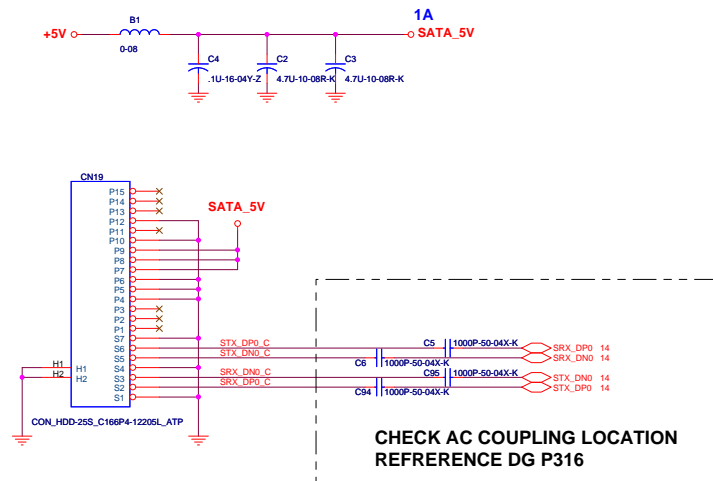




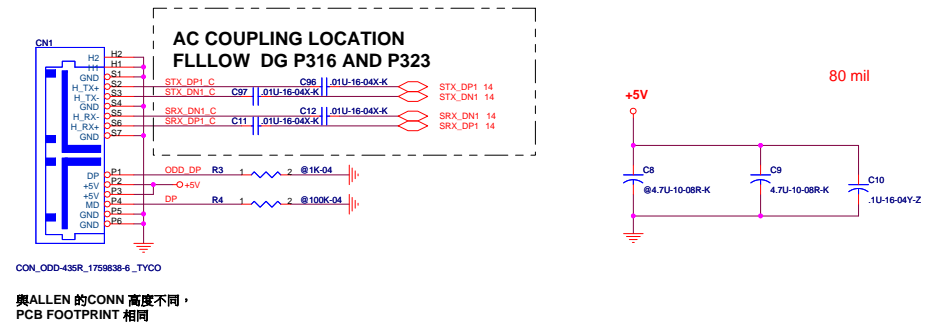




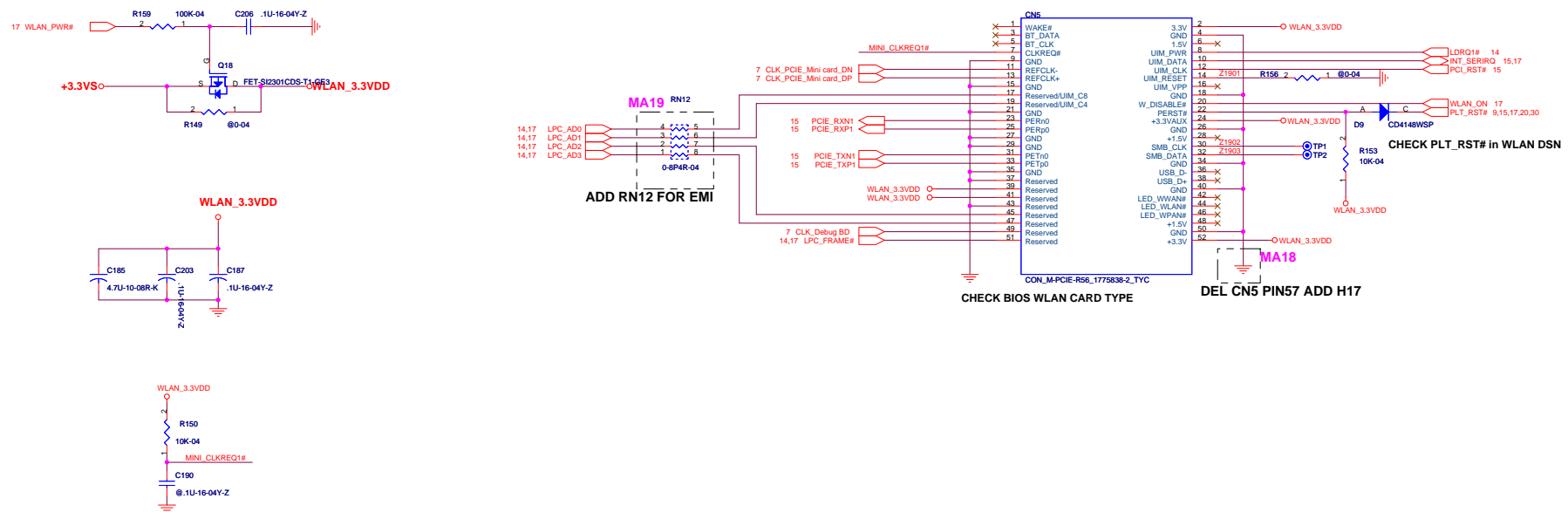
SATA-HDD



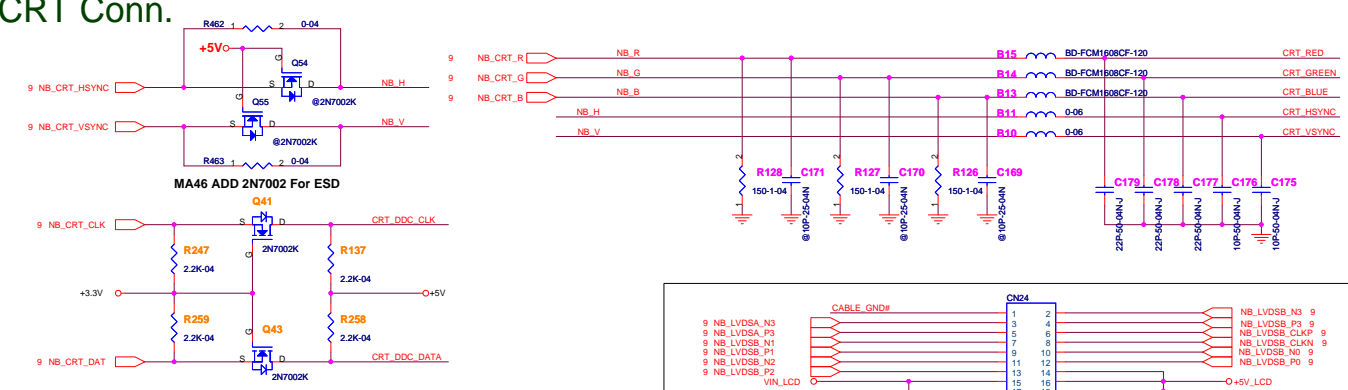
CR-ROM



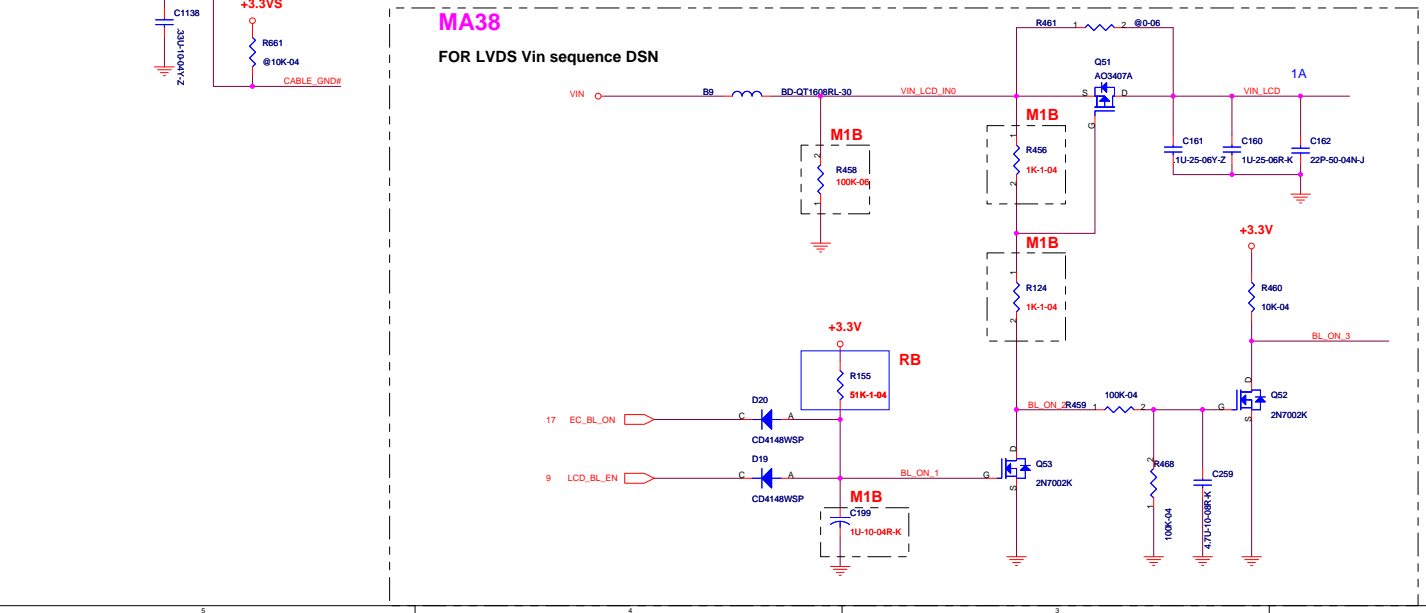
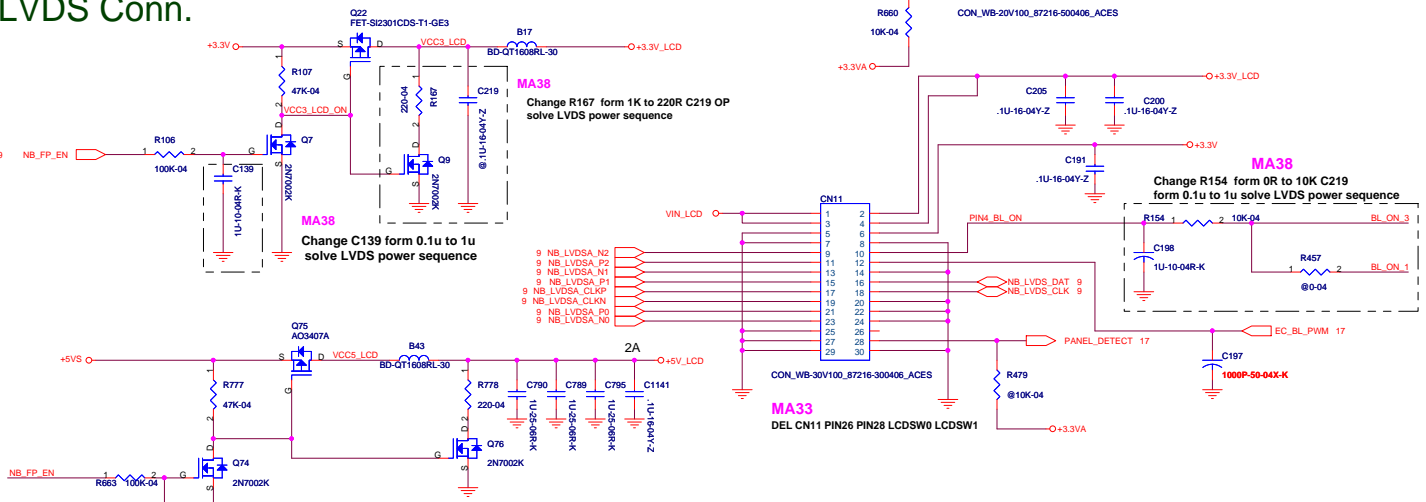
MINI CARD CONN



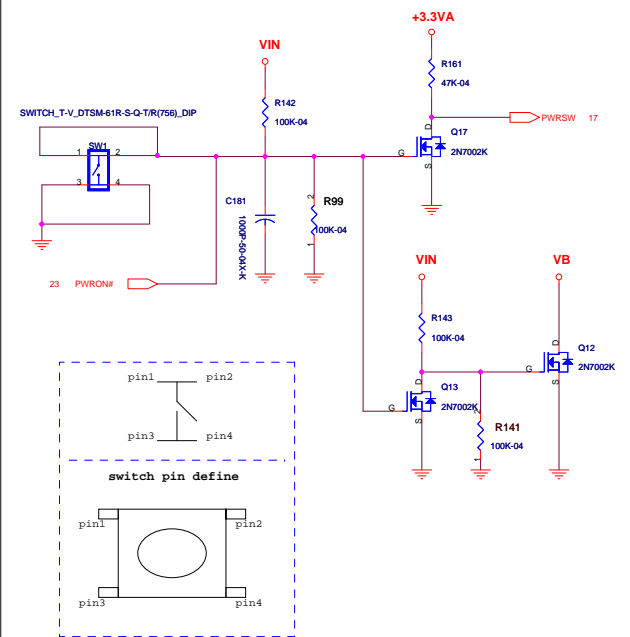
CRT Conn.

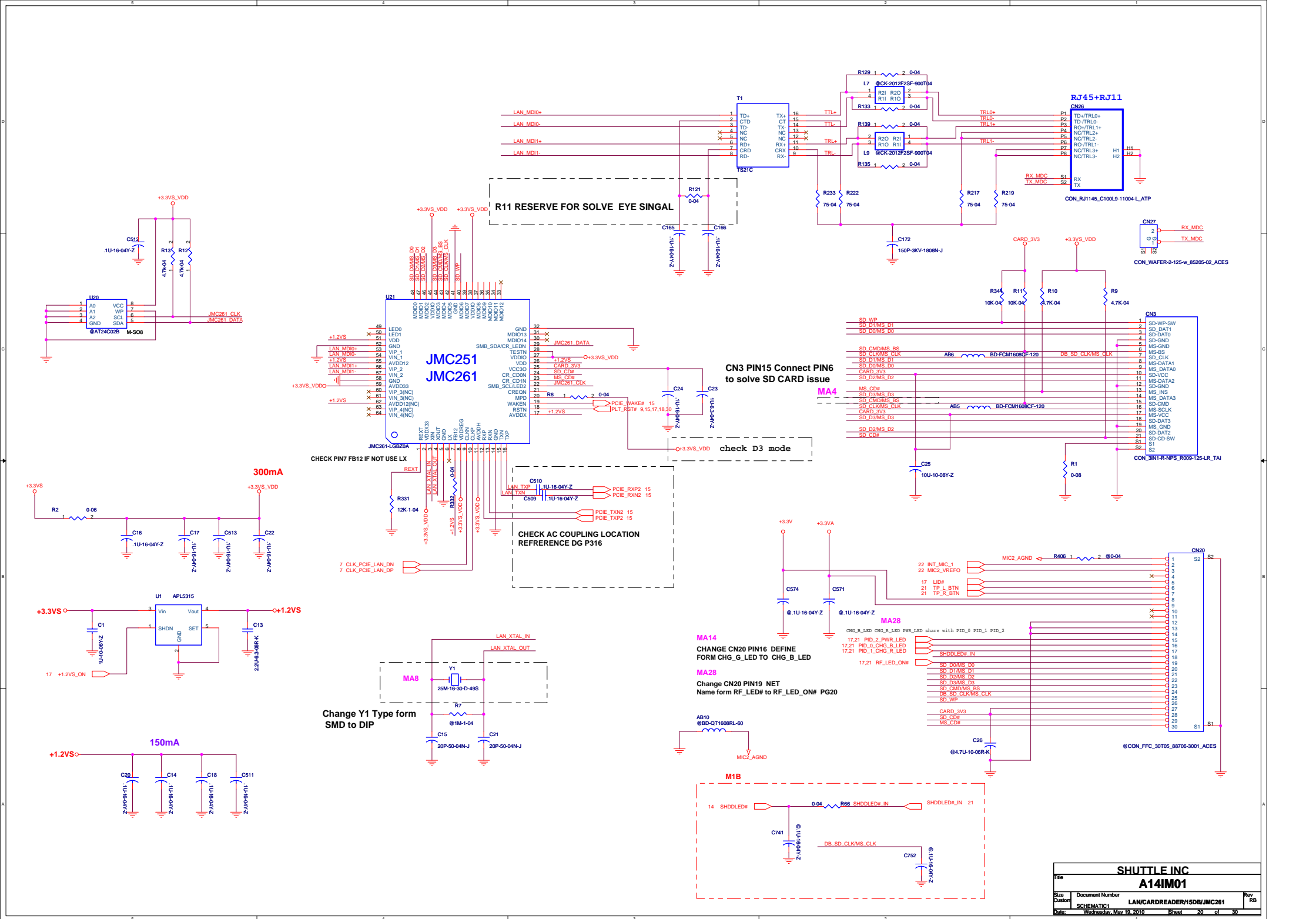


LVDS Conn.

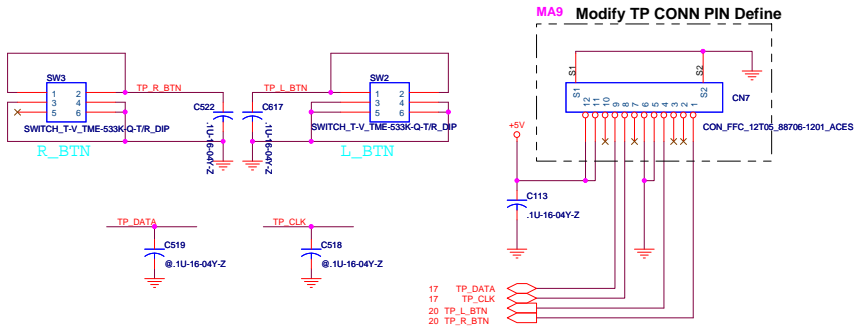


PWR SW

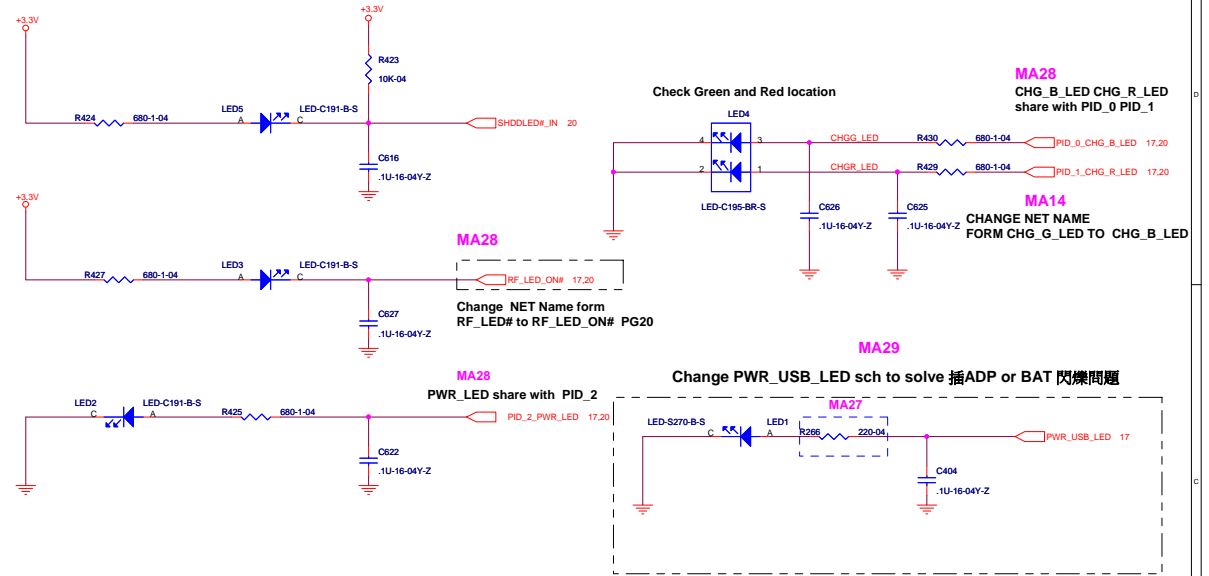




Touch Pad

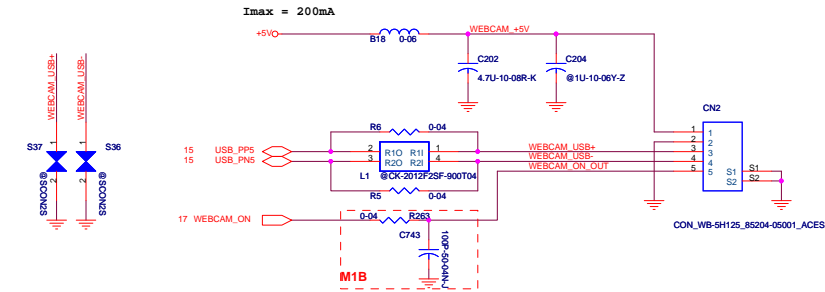


LED MA27 - R424,R427,R425,R430,R429,R266 Change to 220-04

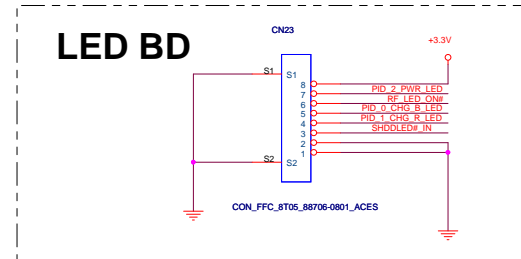


WEBCAM CON

WEBCAM_ON	
1	ON
0	OFF

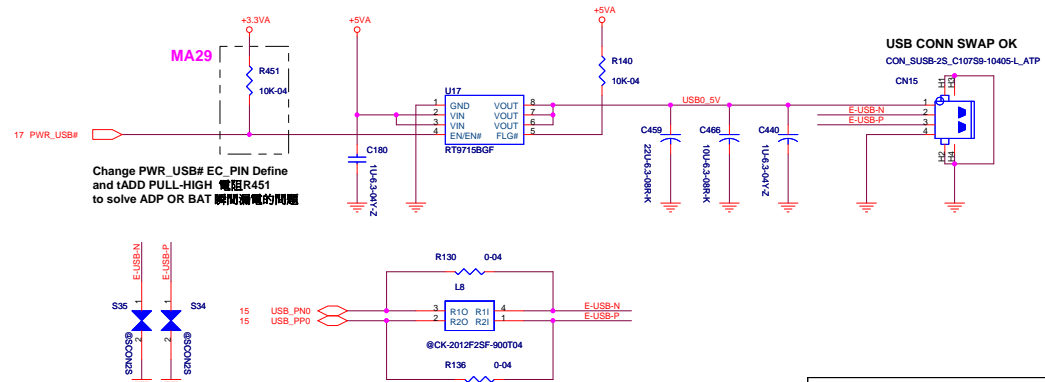


LED BD



- MA14 ADD LED CONN CN23
- MA28 Change CN23 PIN7 NET Name form RF_LED# to RF_LED_ON# PG20
- CHG_B_LED CHG_R_LED PWR_LED share with PID_0 PID_1 PID_2
- MA14 CHANGE CN23 PIN5 DEFINE FORM CHG_G_LED TO CHG_B_LED

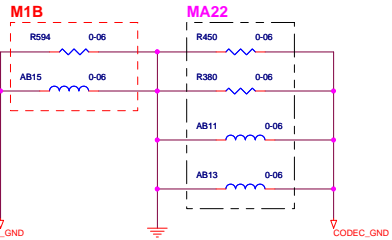
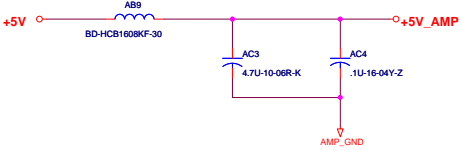
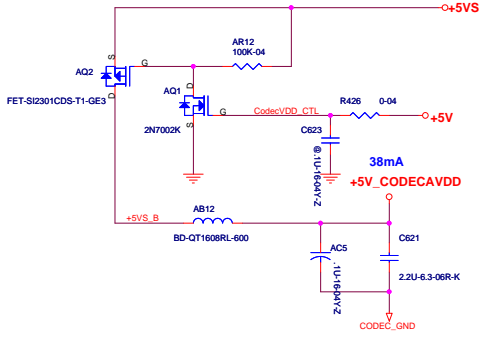
ENHANCE USB Port



SHUTTLE INC			
A14IM01			
File	Document Number	Rev	RB
Size	Custom	TP/LED/WEBCAM/USB CHARGER	
Date	Wednesday, May 19, 2010	Sheet	21 of 30

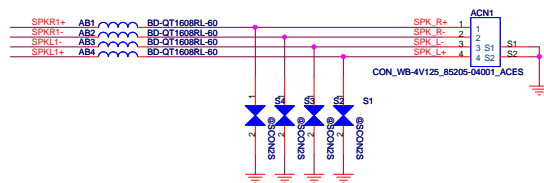
CODEC 92HD81

AMP VDD

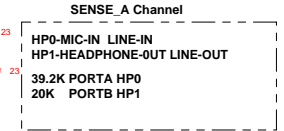
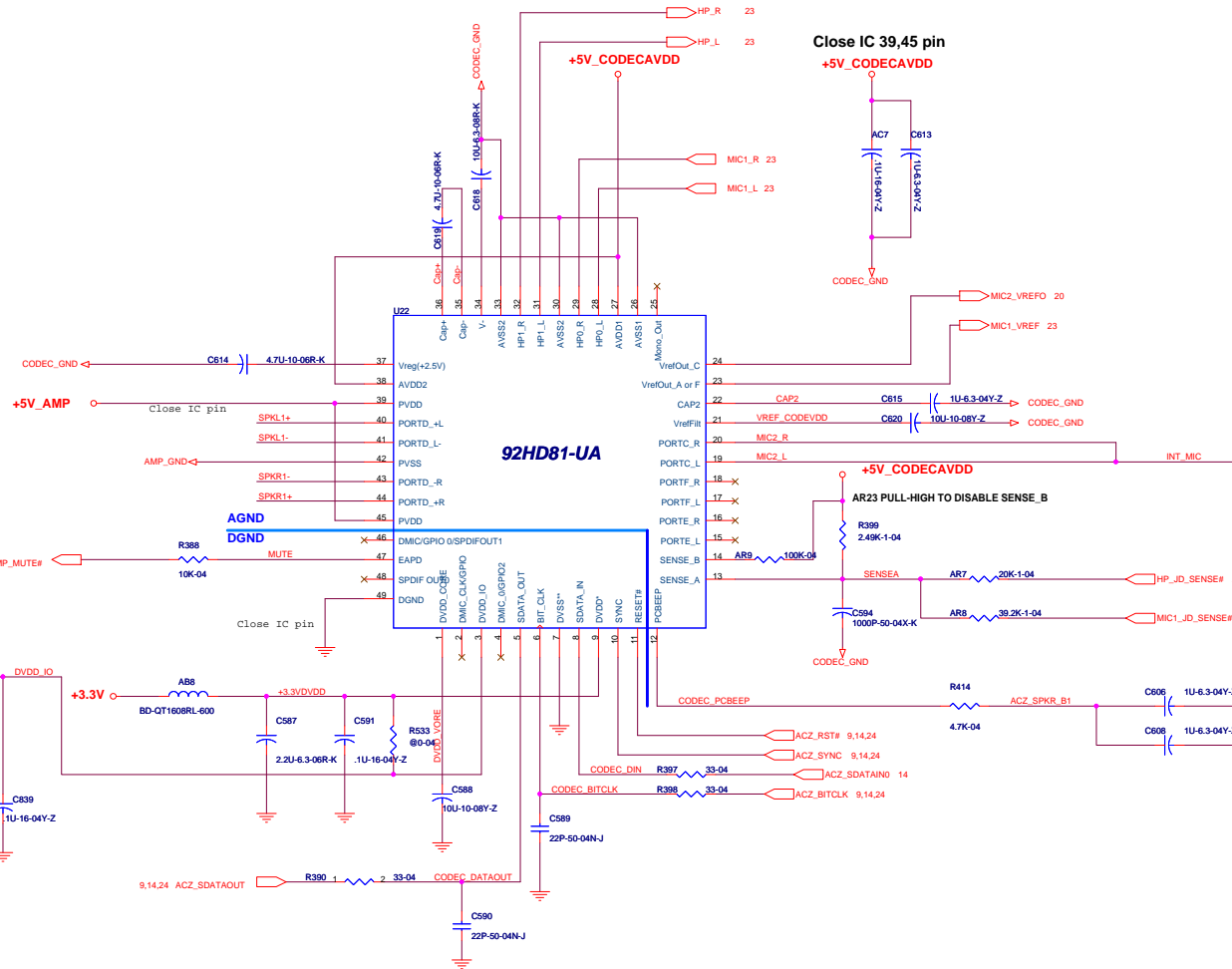
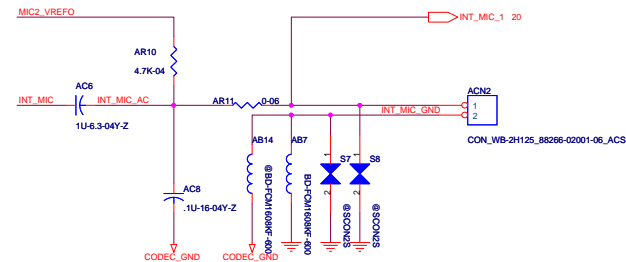


CHANGE R450,R380,AB11,AB13 to 0ohm for EMI

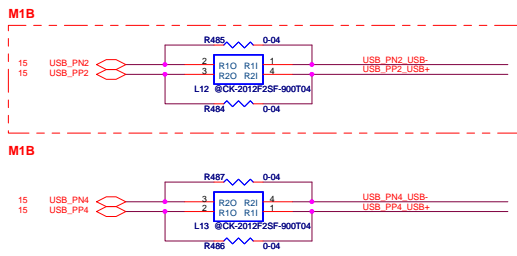
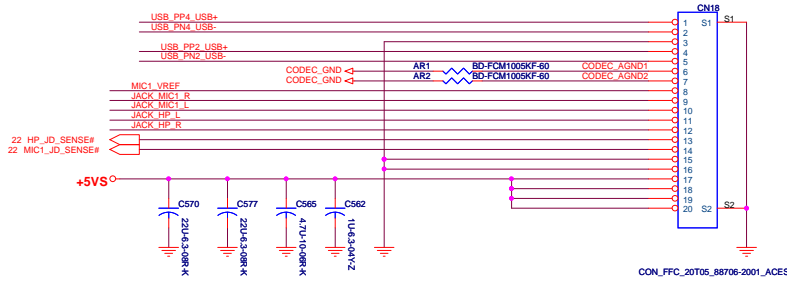
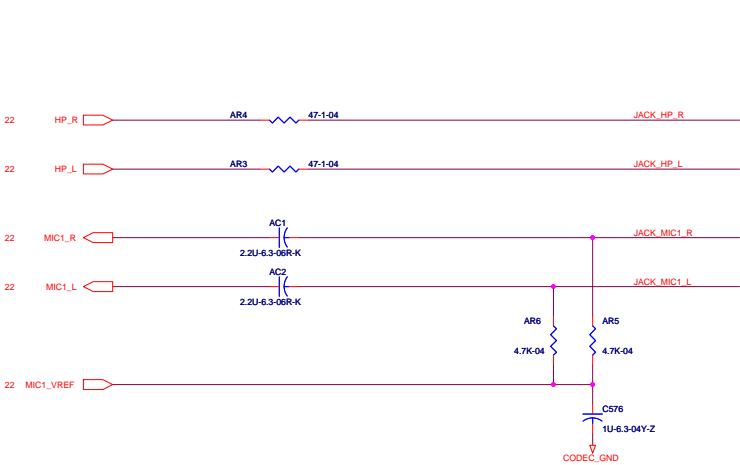
INT_SPEAKER



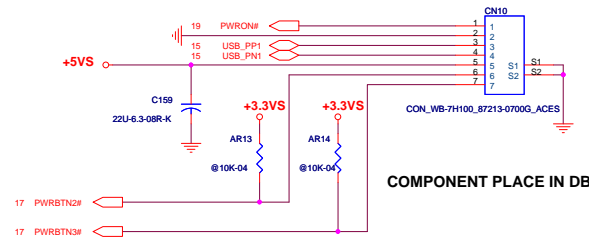
INT_MIC



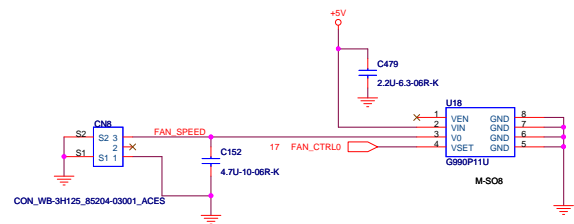
EXT MIC/EXT Line In/ EXT USB JACK



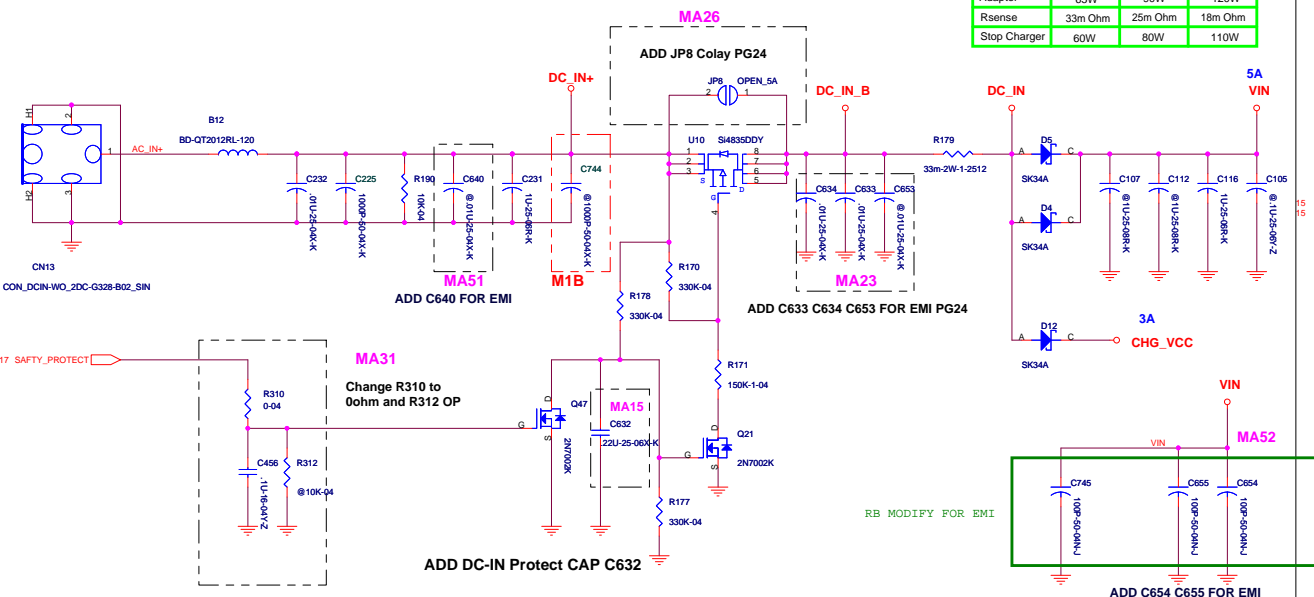
EXT USB PORT 4



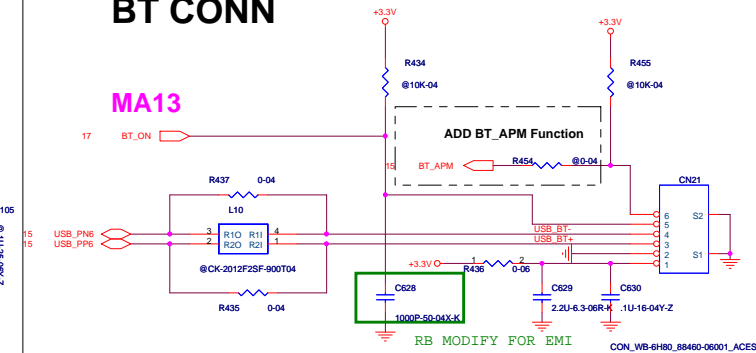
CPU FAN CONTROL



DC IN

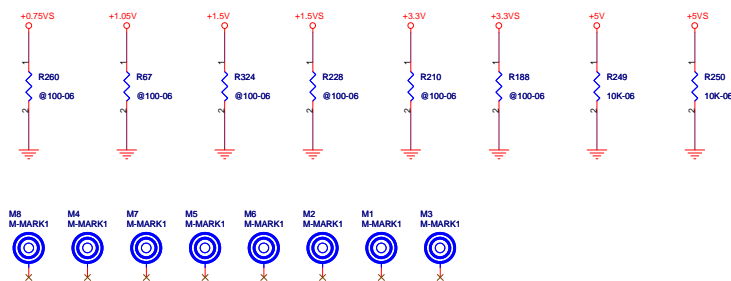


BT CONN

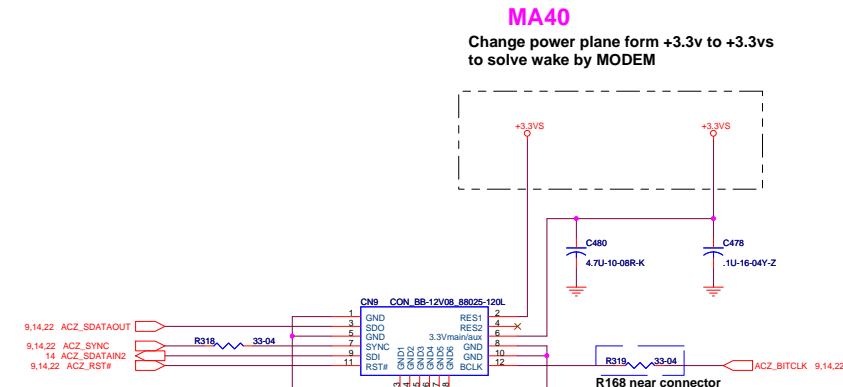


CHECK BT TYPE AND Life power function

Discharge Resistor



MDC



VID: 0.8~1.175V
Icc max: 40A
LLS: set to 2.1mV/A

ADD R432 Pull-High to +3.3V in DELAY_VR_PWRGOOD solve open issue

B16 上件, JP2 OPEN FOR EMI

CHECK BATTERY Leacking current

MA45 ADD C641 C642 FOR EMI

OCP:50A

MA45 Change C201 to 0402 type

DEL-CSN-Connect to GND NET

MA45 ADD JP9 FOR EMI

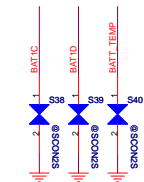
Change C215 Location BY O2

VID TABLE

	6	5	4	3	2	1	0	Vcore	Status
0	0	0	1	0	0	0	0	1.2875	(HFM)
0	0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	0	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	1	0.0000	Shut down

Output Voltage = [Vref x R2/(R1+R2)] x 2



[illegible]
$$\text{Vichg} = \text{RAD1} * \text{Irsense} * 10$$


The diagram shows the connection for Pin 2 of the MA36 module. A blue box labeled 'H1' contains pins 1 through 7. Pin 2 is connected to a red wire labeled 'CON_BAT_M7_C144BN-107A8-L_ATP'. Below the module, a red wire is connected to a ground symbol (a triangle with a horizontal line) labeled '4'. The text 'MA36 CHANGE BATT PIN2 GND Form Battery to DGND' is written in red.

The diagram shows two separate voltage divider circuits. The first circuit for the **BAT_V** pin uses a **BAT+** supply, a 331K-0.1-04 resistor (R162), a 133K-0.1-04 resistor (R169), and a 1U-10-04R-QD45 capacitor (C420) to divide the voltage. The second circuit for the **SENBAT_V** pin uses a **BAT+** supply, a 100K-04 resistor (R163), a 1K-1-04 resistor (R311), and a 1U-10-08V-Z capacitor (C450) to divide the voltage. Both circuits include 2N7002K MOSFETs (Q46 and Q45) connected to ground.

BAT+

R162
331K-0.1-04

R169
133K-0.1-04

C420
1U-10-04R-QD45

Q46
2N7002K

BAT_V 17

BAT+ V_CN#

BAT+

R163
100K-04

Q45
2N7002K

R311
1K-1-04

R309
220K-04

C450
1U-10-08V-Z

SENBAT_V 17

17.6V->BAT_V=2.2V
16.8V->BAT_V=2.1V
13.2V->BAT_V=1.65V
12.6V->BAT_V=1.575V
9.0V->BAT_V=1.125V

Charge / Discharge Detect

The schematic diagram illustrates the Charge / Discharge Detect circuit. It features a voltage divider consisting of resistors R48 (20K-1-04) and R53 (1.5K-1-04) connected to the CHG_REF input. A capacitor C62 (1U-6.3-04Y-Z) is connected to the non-inverting input of the op-amp (U11A, GS358SF). A diode D10 (UDZSNPTE-173.3B) is connected to the non-inverting input. The op-amp is configured as a voltage follower, with its output connected to BAT_1. The op-amp is powered by VIN and GND. The circuit is labeled "CLOSE EC PIN".

CH7318C LEVEL SHIFTER.

